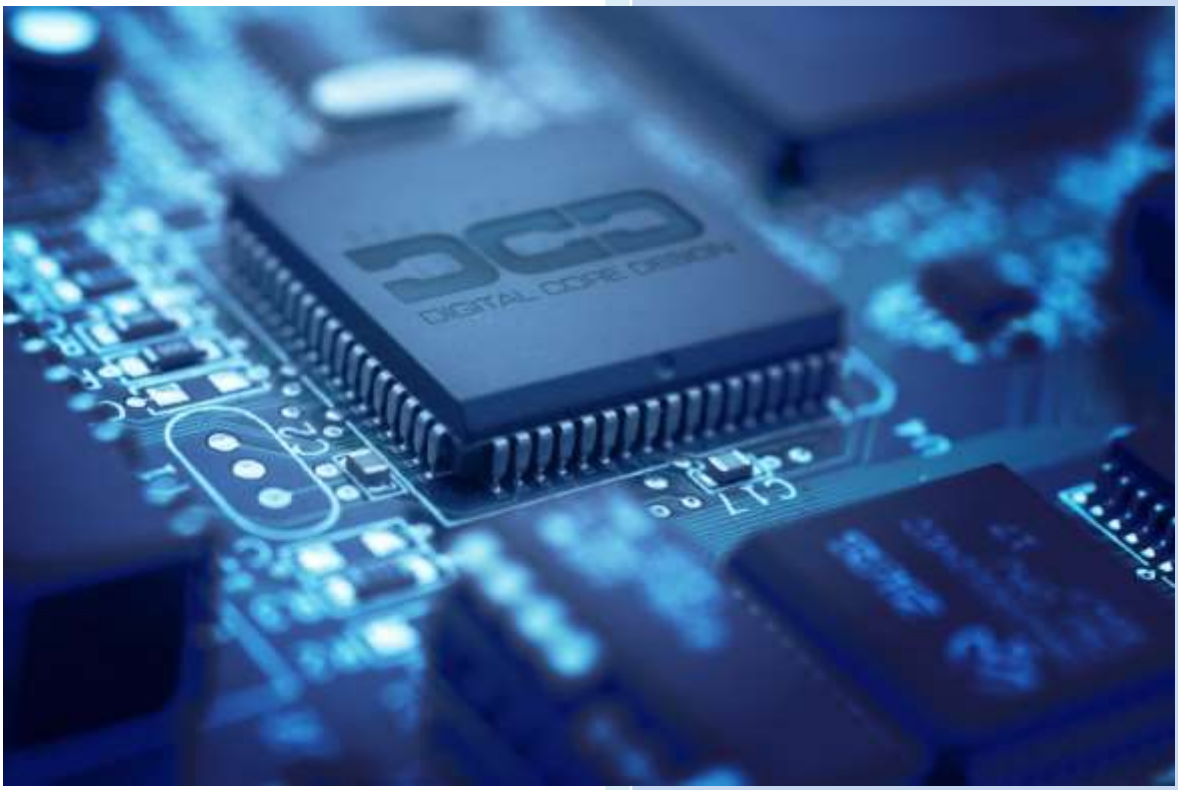
DIGITAL CORE DESIGN

2017

DRPIC1655X IP Core



High Performance 8-bit RISC Microcontroller v. 2.17

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DRPIC1655X is a **low-cost**, **high performance**, 8-bit, fully static soft IP Core, intended to operate with fast, dual ported memory. The core has been designed with a special concern about low power consumption, assuring **best power use, price and performance combination** available on the market. The DRPIC1655X is software-compatible with industry standard PIC 16XXX Microcontrollers. It implements an **enhanced Harvard architecture** (separate instruction and data memories), with independent address and data buses. The 14 bit program memory and 8-bit dual port data memory allow instruction fetch and data operations to occur simultaneously. The instruction fetch and memory transfers can be overlapped by a multi stage pipeline, so that the next instruction can be fetched from a program memory, while the current instruction is executed with data from the data memory. The DRPIC1655X is **4 times faster compared to a standard architecture**. Most instructions are executed within 1 system clock period, except the instructions, which operate directly on a PC (GOTO, CALL, RETURN) program counter. This situation requires the pipeline to be cleared and subsequently refilled. This operation takes an additional clock cycle. The DRPIC1655X fits in applications ranging from high-speed automotive and appliance motor control, to low-power remote transmitters/receivers, pointing devices and telecom processors. A built-in power save mode makes this IP core perfect for applications, where the power consumption aspect is critical. The DRPIC165X is delivered with **fully automated test bench** and **complete set of tests**. Each of our PIC Cores has a built-in support for DCD's Hardware Debug System called **DoCD™**. It is a **real-time hardware debugger**, which provides debugging capability of a whole System on Chip (SoC).

PERIPHERALS

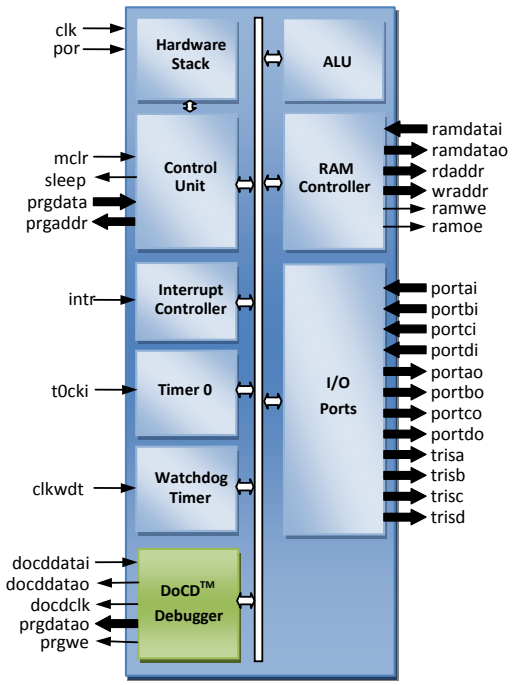
- Four 8 bit I/O ports
  - *Four 8-bit corresponding TRIS registers*
  - *Interrupt feature on PORTB(7:4) change*
- Timer 0
  - *8-bit timer/counter*
  - *Readable and Writable*
  - *8-bit software programmable prescaler*
  - *Internal or external clock select*
  - *Interrupt generation on timer overflow*
  - *Edge select for external clock*
- Watchdog Timer
  - *Configurable Time out period*
  - *7-bit software programmable prescaler*
  - *Dedicated independent Watchdog Clock input*
- Extended Interrupt Controller
  - *Three individually maskable Interrupt sources*
    - *External interrupt INT*
    - *Timer Overflow interrupt*
    - *Port B[7:4] change interrupt*
- DoCD™ debug unit
  - *Processor execution control*
    - *Run*
    - *Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Data Memory*
    - *Special Function Registers (SFRs)*
    - *Hardware Stack and Stack Pointer*
  - *Hardware execution breakpoints*
    - *Program Memory*
    - *Data Memory*
    - *Special Function Registers (SFRs)*
  - *Three wire communication interface*

OPTIONAL PERIPHERALS

Optional peripherals (not included in the presented DRPIC1655X Microcontroller Core) are also available. The optional peripherals can be implemented upon customer's request.

- Timer 1 and Timer 2
- Full duplex UART
- SPI – Master and Slave Serial Peripheral Interface
  - *Supports speeds up ¼ of system clock*
    - *Mode fault error*
    - *Write collision error*
  - *Software selectable polarity and phase of serial clock SCK*
  - *System errors detection*
  - *Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)*
  - *Interrupt generation*
- PWM – Pulse Width Modulation Timer
  - *2 independent 8-bit PWM channels, concatenated on one 16-bit PWM channel*
  - *Software-selectable duty from 0% to 100% and pulse period*
  - *Software-selectable polarity of output waveform*
- I2C bus controller - Master
  - *7-bit and 10-bit addressing modes*
  - *NORMAL, FAST, HIGH speeds*
  - *Multi-master systems supported*
  - *Clock arbitration and synchronization*
  - *User defined timings on I2C lines*
  - *Wide range of system clock frequencies*
- I2C bus controller - Slave
  - *NORMAL, FAST and HIGH Speed modes*
  - *Wide range of system clock frequencies*
  - *User defined data setup time on I2C lines*

BLOCK DIAGRAM



CPU FEATURES

- Software compatible with the PIC16C55X industry standard
- Hardware on Chip debugger – DoCD™
- Pipelined Harvard architecture 4 times faster compared to original implementation
- 35 instructions
- 14 bit wide instruction word
- Up to 32 K bytes of Data Memory
- Up to 64K bytes of Program Memory
- Configurable hardware stack
- Power saving SLEEP mode
- Fully synthesizable, static synchronous design with no internal tri-states
- Technology independent HDL Source Code
- **1.4 GHz virtual** clock frequency in a 0.18u technological process

LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

CONFIGURATION

The following parameters of the DRPIC1655X core can be easily adjusted to requirements of dedicated application and technology. Configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

• Number of hardware stack levels	- 1-16 - default 8
• Memories type	- synchronous - asynchronous
• RAM extension	- 32 KB - 512 B - default
• SLEEP mode	- used - unused
• WATCHDOG Timer	- used / width - unused
• Timer system	- used - unused
• Interrupt system	- used - unused
• PORTS A,B,C,D	- used - unused
• DoCD™ Debug Unit	- used - unused

PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
clkwdt	input	Watchdog clock
por	input	Global reset Power On Reset
mclr	input	User reset
prgdata[13:0]	input	Data bus from program memory
ramdatai[7:0]	input	Data bus from int. data memory
intr	input	External interrupt
t0cki	input	Timer 0 input
portxi[7:0]	input	Port A, B, C, D input
docddatai	input	DoCD™ Debugger input
prgaddr[15:0]	output	Program memory address bus
ramdatao[7:0]	output	Data bus for internal data memory
rdaddr[14:0]	output	RAM read address bus
wraddr[14:0]	output	RAM write address bus
ramwe	output	Data memory write
ramoe	output	Data memory output enable
sleep	output	Sleep signal
portxo[7:0]	output	Port A, B, C, D outputs
trisx[7:0]	output	Ports A, B, C, D data direction pins
docddatao	output	DoCD™ Debugger data output
docdclk	output	DoCD™ Clock line
prgdatao[13:0]	output	Program Memory data output
prgwe	output	Program Memory write enable

UNITS SUMMARY

ALU – Arithmetic Logic Unit - performs arithmetic and logic operations during execution of an instruction. This module contains work register (W) and Status register.

Control Unit – It performs the core synchronization and data flow control. This module manages execution of all instructions. It carries out decode and control functions for all other blocks. It contains program counter (PC) and hardware stack.

Hardware Stack – It's a configurable hardware stack. The stack space is not a part of either program or data space and the stack pointer is neither readable, nor writable. The PC is pushed onto the stack, when CALL instruction is executed or an interrupt causes a branch. The stack is popped, while RETURN, RETFIE and RETLW instruction is executed. The stack operates, as a circular buffer - this means, that after the stack has been pushed eight

times, the ninth push overwrites the value, that was stored from the first push.

RAM Controller – It performs interface functions between Data Memory and DRPIC16XXX internal logic. It assures correct Data Memory addressing and data transfers. The DRPIC16XXX supports two addressing modes: direct or indirect. In Direct Addressing, the 9-bit direct address is computed from RP(1:0) bits (STATUS) and from 7 least significant bits of instruction word. Indirect addressing is possible, by using the INDF register. Any instruction using INDF register, actually accesses data pointed to by the FSR (file select register). Reading INDF register indirectly, will produce 00h. Writing to the INDF register indirectly, results in a nonoperation. An effective 9-bit address is obtained, by concatenating the IRP bit (STATUS) and the 8-bit FSR register.

Interrupt Controller – Interrupt Controller module is responsible for interrupt manage system for the external and internal interrupt sources. It contains interrupt related register, called INTCON. There are three interrupt sources:

- External interrupt INT
- TMR0 overflow interrupt
- PORTB change interrupt (pins B[7:4])

INTCON records individual interrupt requests in flag bits. A global interrupt enable (GIE) bit enables all unmasked interrupts. Each interrupt source has an individual enable bit, which can enable or disable corresponding interrupt. When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. The interrupt flag bits must be cleared in software before re-enabling interrupts.

Timer 0 – Main system's timer and prescaler, operates in two modes: 8-bit timer or 8-bit counter. In the "timer mode", timer/prescaler registers are incremented in every instruction cycle (1 or 2 CLK periods). When the prescaler is assigned into the TIMER, prescaler ratio can be divided by 2, 4, ..., 256. In the "counter mode", the timer register is incremented in every falling or rising edge of T0CKI pin, depending on T0SE bit in OPTION register.

Watchdog Timer– The watchdog timer is a free running timer. WDT has its own clock input, separate from system clock. It means, that the WDT will run, even if the system clock is stopped by execution of SLEEP instruction. During normal operation, a WDT timeout generates a Watchdog reset. If the device is in SLEEP mode, the WDT timeout causes the device to wake-up and continue with normal operation.

I/O Ports – The ports block contains general purpose I/O ports and data direction registers (TRIS). The DRPIC16XXX has four 8-bit full bi-directional ports PORT A, PORT B, PORT C, PORT D. Each port's bit can be individually accessed, by bit addressable instructions. Read and write accesses to the I/O port, are performed via their corresponding SFR's PORTA, PORTB, PORTC, PORTD. The reading instruction, always reads the status of Port pins. Writing instructions always write into the Port latches. Each port's pin has a corresponding bit in TRISA, B, C and D registers. When the bit of TRIS register is set, it means, that the corresponding bit of port is configured as an input (output drivers are set into the High Impedance).

DoCD™ Debug Unit – a **real-time hardware debugger,** which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurred at particular address, with certain data pattern or without pattern. The **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core, in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

ARCHITECTURE IMPROVEMENT

Most instruction of DRPIC1655X is executed within 1 CLK period, except program branches, that require 2 CLK periods. The table below shows sample instructions execution times:

Mnemonic operands	DRPIC1655X (CLK cycles)	PIC16C554 (CLK cycles)	Impr.
ADDWF	1	4	4
ANDWF	1	4	4
RLF	1	4	4
BCF	1	4	4
DECFSZ	1(2)[1]	4(8)[1]	4
INCFSZ	1(2)[1]	4(8)[1]	4
BTFSC	1(2)[1]	4(8)[1]	4
BTFSS	1(2)[1]	4(8)[1]	4
CALL	2	8	4
GOTO	2	8	4
RETFIE	2	8	4
RETLW	2	8	4
RETURN	2	8	4

[1] **number of clock in case when result of operation is 0.**

DFPIC&DRPIC FAMILY OVERVIEW

The family of DCD DFPICXX & DRPICXX IP Cores combines high–performance, low cost, and small compact size, offering best price/performance ratio in the IP Market. DCD's Cores are designed to be used in cost-sensitive consumer products, computer peripherals, office automation, automotive control systems, security and telecommunication applications. DCD's DFPICXX & DRPICXX IP Cores family contains four 8-bit microcontroller Cores to meet your needs in the best way: DFPIC165X 12-bit program word, DFPIC1655X 14-bit program word, and also DRPIC1655X and DRPIC177X single cycle microcontrollers with 14-bit program word. All three microcontroller cores are binary compatible with widely accepted PIC16C5X and PIC16CXXX. They have modified RISC architectures, two or four times faster than the original ones. The DFPICXXX & DRPICXX IP Cores are written in pure VHDL/VERILOG HDL languages, which makes them technologically independent. All of the DFPICXX & DRPICXX family members are supported by a power saving SLEEP mode, which allows the user to configure the watchdog time-out period and a number of hardware stack levels. DFPICXX & DRPICXX can be fully customized, according to the customer requirements.

Design	Program Memory space	Program word length	Data Memory space	RAM extension to 32kB	Number of instructions	I/O Ports	Timer 0	Timer 1	Timer 2	Watchdog Timer	CCP1	USART	Sleep Mode	External interrupts	Internal Interrupts	Wake up on port pin change	Speed rate	DoCD™ Debugger	Size (gate)
DFPIC165X	2k	12	128	-	33	24	✓	-	-	✓	-	-	✓	-	-	-	2	-	2 700
DFPIC1655X	64k	14	512	✓	35	16	✓	-	-	✓	-	-	✓	5	1	✓	2	✓*	3 900
DFPIC166X	64k	14	512	✓	35	32	✓	✓	✓	✓	✓	✓	✓	5	5	✓	2	✓*	6 000
DRPIC1655X	64k	14	512	✓	35	32	✓	-	-	✓	-	-	✓	5	1	✓	4	✓*	4 800
DRPIC166X	64k	14	512	✓	35	32	✓	✓	✓	✓	✓	✓	✓	5	5	✓	4	✓*	6 700

DFPIC & DRPIC family of High Performance Microcontroller Cores

**** Optional***

PERFORMANCE

The following table gives a survey about the Core area and performance in INTEL FPGA® devices after Place & Route:

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6	921	111 MHz
CYCLONE	-6	923	107 MHz
STRATIX	-5	922	114 MHz
STRATIX II	-3	823	189 MHz
STRATIX GX	-5	922	116 MHz
APEX II	-5	1131	94 MHz
APEX20KC	-7	1131	81 MHz
APEX20KE	-1	1131	70 MHz
APEX20K	-1	1131	41 MHz
ACEX1K	-1	1150	64 MHz
FLEX10KE	-1	1150	59 MHz

Core performance in INTEL FPGA® devices

Area utilized by the each unit of DRPIC1655X core in vendor specific technologies is summarized in the table below.

Component	AREA [LC]	AREA [FFs]
CPU*	711	285
Timer 0	60	29
Watchdog Timer	55	38
I/O Ports	96	64
Total area	**922**	**416**

Core components area utilization - CYCLONE

***CPU – consisted of ALU, Control Unit, Bus Controller, Hardware Stack, Extended interrupt controller, External INT pin Interrupt Controller, Extended Interrupt controller, 512 B of RAM 8kW of program memory**

CONTACT

Digital Core Design Headquarters:

Wroclawska 94, 41-902 Bytom, POLAND

e-mail: info@dcd.pl
tel.: 0048 32 282 82 66
fax: 0048 32 282 74 37

Distributors:

Please check: http://dcd.pl/sales